**Motivation: Low–k** dielectrics are used as insulators to decrease the parasitic RC delays such as Cross talk, Signal Delays, and power consumption. **to achieve low–k :** (𝜀−1)/(𝜀+2)=(1/3𝜀0)Σ𝑁𝑗𝛼𝑗 ; Nj: Density of the material: number of atoms. αj: Polarizability of the combination of the material used ; *Nj, αj, should be very low in order to achieve the low–k.* The existed dielectric SiO2 has a huge polarizability and density hence its k value stays between 3.9 ~4.4 which is normal k, low–k is even lower than that; Ultra low–k stands less than 2.5.



**Type of process used:**

PECVD (Plasma Enhanced Chemical Vapor Deposition) porogen approach, deposition from the decomposition of (at least) two precursors in the plasma.

**Precursors:** Pure organic molecule (porogen) & Organo-Silicon (Matrix Precursor)

**Process Flow:** Post-deposition treatment (curing) for porogen removal & Cross Linking

Formation of a hybrid film composed of *Organo-Silicate-based matrix* enclosing organo inclusions.

**Example:** Thermal annealing

➔ Film becomes Porous + Ultra Low–k

**Film Properties affected:** Mechanical stability (E, H) Porosity / density (optical – R.I)



**Chemical Mechanical Planarization (CMP)** is mechanically enhanced chemical etching or chemically enhanced mechanical grinding to planarize surfaces by removing unwantedly present material after some other process steps.

**Capabilities of CMP:** • Can planarize surfaces by removal of materials such that topography is eliminated, or material is left at defined areas. • CMP provides local and global planarity • CMP enables indirect patterning due to an adjustable polish selectivity between different materials.

**Example Applications:** • STI Formation • Tungsten plug formation • Deep trench capacitor • Cu dual damascene

**Consumables in CMP:** • Slurries • Pads • Brushes and Conditioner

Shape

Description automatically generated100%step coverage-ALD,CVD

Advanced sputtering tech— Collimated Sputtering, Long through sputtering, Ionised metal deposition

![Table

Description automatically generated]()

![Chart, treemap chart

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**Basic process steps (BPS):** • Indivisible step in the process flow • Characterized by physical / chemical parameters (Temperature, pressure, gas composition…) **Example:** Special diffusion step (pre-deposition), implantation step, special cleaning step (rinsing)

**Process:** • Consists of one or more BPS • Carried out by using specific tools (equipment) • Standardized component of technology • Results in achievement of a specific property **Example:** doping (pre-deposition, drive in), photolithography (deposition of resist, exposure, development, ….)

**Basic Technology:** • Sum of processes (or BPS) to be performed for the fabrication of a specific product **Example:** CMOS, BICMOS, Bipolar….

**Process Technology:** • Physical, chemical and other mechanism/ principle of the process • Technical realization using specific equipment • Process integration issues

**Name four basic MOS transistor types : NMOS Enhancement type ; NMOS Depletion type ; pMOS Enhancement type ; pMOS Depletion type**

**Name important trends in transistor types**. • Production of many identical devices / circuits / chips by one process, Cost decrease!

• Characteristic Quantities: – Wafer diameter(size) increase **1. Die size increase 2.** Number of transistors per die (degree of integration) **3. Yield**

**• Main features:** • New and improved products (Performance & Reliability) •Continuous increase of the degree of integration • Scaling down – miniaturization, decrease of lateral dimensions and layer thickness • Goal: equal or higher yield than in previous technology node

**Geometrical Scaling: (Constant field)** Refers to the continued shrinking of horizontal and vertical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.

**Equivalent scaling: (Occurs in conjunction with, also enables, continued geometrical scaling)** Refers to 3-dimensional device structure (“Design Factor”) improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.

**Design Equivalent scaling : (Occurs in conjunction with equivalent scaling and continued geometric scaling)** Refers to design technologies that enable high performance, low power, high reliability, low cost, and high design productivity. **Examples for Equivalent scaling:** low–k/Cu, HKMG, electrostatic control (SOI), new channel materials, strain engineering/ stressors.

**Front End** – Wafer level fabrication process for active devices & Interconnects **Or** the combination of front end of line (being fabrication of transistors including local interconnects) and back end of line (the fabrication of connection systems including passivation band path metallization) **Back end** – Packaging

**More’s Law:** Moore’s law states that the number of transistors incorporated in a chip will approximately double every 24 months. **More Moore:** Decrease of all characteristic dimensions and structures (Ex: Channel length of MOS transistors) **More than Moore:** Integration of various sensors and actuators with the miniaturized(micro) electronics.

Name five basic process steps of CMOS Technology: • SiO2 oxide layer formation on the wafer surface (usually on P type Si Substrate) • Photoresist coating on oxide layer and masking • Etching followed by Acidic etching and then the removal of photo resist • Implantation or diffusion to form n and p type regions. • Removal of unwanted material • Polysilicon deposition and metallization

3D-inlegraton implies any Stacking of integrated devices (ICs, MEMS)their vertical and electrical connection in order to increased integration density; increased performance; more functionality; reduced power consumption; minimum volume and weight, mixed technologies; 3d SoC

*193nm immersion lithography* is used in 32/28nm technology nodes.

𝐼𝑚𝑖𝑛=(𝐾1×𝜆)/𝑁𝐴 𝐾1 – Rayleigh limit; 𝜆 –𝑊𝑎𝑣𝑒𝑙𝑒𝑛𝑔𝑡ℎ; NA: Numerical Aperture

**3 Ways to increase Imin: I. Reduce 𝜆 II.** Increase NA (Immersion-Litho) **III.** Reduce 𝐾1(RET)

• 3 resolution enhancement techniques: **I.** Optical proximity correction (OPC) **II.** Off-axis illumination (OAI) **III. Phase shift masks (PSM) IV.** Double exposure / double patterning (DA)

**Name the process modules of conventional (Si-gate, Si bulk CMOS Technology Front End Process flow in the Right Sequence**



